

Strain-engineering in thin Si_{1-x}Ge_x layers on mesa epitaxy

Ismail Madaci^a, Isabelle Berbezier^a, Luc Favre^a, Kennet D. R. Hannikainen^{a, b},
Olivier Gourhant^c, Fabien Deprat^c, Jean-Noël Aqua^b

^a Aix Marseille Université, CNRS, Université de Toulon, IM2NP, Avenue Escadrille Normandie
Niemen, 13397, Marseille, France

^b Sorbonne Université, Centre National de la Recherche Scientifique, Institut des NanoSciences de
Paris, INSP, 4 place Jussieu, F-75005, Paris, France

^c ST-Microelectronics, 850 Rue Jean Monnet, 38920, Crolles, France

Corresponding author email: ismail.madaci@im2np.fr

Commonly used as Source/Drain stressors in the MOSFET devices, strained Silicon-Germanium (Si_{1-x}Ge_x) layers also demonstrate their effectiveness through the incorporation in MOSFETs channels, significantly increasing hole/electron mobility and enhancing the overall performance of these devices^{1,2}. In this communication, we present a coupled theoretical/experimental study looking into the intricate interplay of finite-size effects and elastic strain relaxation in strained epitaxial SiGe nanolayers (Si_{1-x}Ge_x) integrated on small Si gate configurations. As gate dimensions decrease, stress relaxation emerges as a crucial issue impacting hole/electron mobility. Our investigation reveals a unique morphological evolution, distinct from self-induced instability, initiated by elastic inhomogeneity near the free sides of the system. Employing a thermodynamic surface diffusion framework that accounts for elasticity and capillarity, we utilize a two-dimensional Airy formalism to examine growth dynamics. Eigenmode decomposition of the resulting dynamic equation unveils various changes based on the mesa geometric parameters. The dynamics of this evolution depend on the strain inhomogeneity near the free faces, forming a relaxation zone influenced by film thickness and mesa aspect ratio. We show that the evolving shape and speed of the nanolayer exhibit a distinct W or V surface as a function of geometry and time³. This variability reaches a stationary profile when the capillarity and elasticity forces counterbalance. The present work exhibits the experimental validation which corroborates the simulations in specific conditions. As the semiconductor industry continues to push the boundaries of device performance, our findings contribute to the ongoing efforts in optimizing SiGe-based devices for the 28nm node BiCMOS transistors and beyond.

- (1) Ang, K.-W.; Lin, J.; Tung, C.-H.; Balasubramanian, N.; Samudra, G. S.; Yeo, Y.-C. *IEEE Trans. Electron Devices* **2008**, 55 (3), 850–857. <https://doi.org/10.1109/TED.2007.915053>.
- (2) Fitzgerald, E. A.; Lee, M. L.; Leitz, C. W.; Antoniadis, D. A. **2003**. <https://dspace.mit.edu/handle/1721.1/3726>
- (3) Hannikainen, K. D. R.; Deprat, F.; Gourhant, O.; Berbezier, I.; Aqua, J. *Adv Materials Technologies* **2024**, 9 (4), 2301655. <https://doi.org/10.1002/admt.202301655>.